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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,961	04/02/2004	Tan Ba Tran	550-545	7733

23117 7590 04/18/2006

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,961	TRAN ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. 1-3, 5-7, 9-12, 14-15, and 17-18 are rejected under U.S.C. 102(b) as being anticipated by Makris et al. (US Patent 4,979,100).

Claim 1. A data processing apparatus comprising:

- arbitration logic; *(Column 18, lines 25-26 – Mention Arbitration Logic)*
- and a data processor core, said data processor core comprising: a memory access interface portion for performing data transfer operations between an external data source and at least one memory associated with said data processor core; a data processing portion for performing data processing operations; *(Column 4, lines 3-66 – State the following: "Once data is transferred into the main memory 10, CPU 15 monitors that data and the intercard (i.e., LPUs and other units of the switch) communication areas, to determine where the data should now be transferred. The CPU then notifies an appropriate LPU that particular data in the main memory is to be transferred to that LPU. Accordingly, the path of data is via a modem through an LPU, with arbitration onto the bus and into main memory. Then a processing decision is made by the CPU as to the intra-switch destination for the data, and the CPU thereupon notifies the other card (the LPU), whereupon the data is transferred out of main memory through the selected LPU, its associated interface, and out through*

that modem or port. This is the manner in which the TP4000/II switch performs its packet switching. The packetizing (i.e., packet assembly) is accomplished in the LPU. Asynchronous data is received, packets are formed, and the packets are subsequently switched throughout the network until, at the other end, the packet is disassembled and transferred as asynchronous data again. The TP4000/II arbitration protocol on the DAB bus treats CPUs separately from LPUs. A block diagram useful for describing the protocol is shown in FIG. 3. The LPUs 40-1, 40-2, 40-n compete for access to the bus, in order to have their respective data packets (if any) read into the main memory. The competition is arbitrated by ARB unit 42 in a daisy chain approach by which the ARB initially passes a token to the LPU 40-1. If that LPU is ready to use the bus, it will hold the token and the bus, and on completion of its use will pass the token to the next LPU in the chain. If at that point LPU 40-2 has no need for access to the bus, it will simply pass the token to the next LPU. Finally, the last LPU in the chain, 40-n, passes the token back to the ARB 42. The scheme is such that the holder of the token holds possession of the bus. A separate token is employed for the CPUs 45-1 and 45-2, and here again a daisy chain approach is employed for the arbitration. If the CPUs are not using their bus time, the LPUs may use it. With this protocol, there may be passage of considerable time for the token to travel between units before the unit presently desiring to use the bus is encountered. That is, if LPU 40-1, for example, initially receives the token and has no present need to use the bus, the token is passed from LPU to LPU, When perhaps only LPU 40-15 is in need of access. Viewing the bus protocol of FIG. 3 in terms of clock cycles, a CPU or an LPU will remain idle and waiting until the token is passed to it--indeed, the unit may sit and wait until the token passes through a considerable number of LPUs until it finally gets the token--despite the fact that it may be

the only card that is seeking to transfer data and, therefore, that requires the bus. Hence, time, and as a result, valuable bandwidth may be wasted as the token is passed from card to card until a need to use the bus is found. Moreover, as previously noted, at least some of the units within the packet switch, such as the LPUs, are individually configured on respective printed circuit cards. These cards are inserted into designated slots in cages within a console. The bus protocol requires that a ribbon cable be run between cages, with an attendant further slowing of the bus")

- a read/write port for transfering data from said processor core to at least two buses, said at least two buses providing data communication between said processor core and said at least one memory, said at least one memory comprising at least two portions, each of said at least two buses providing data access to respective ones of said at least two portions, *(Column 19, lines 52-58 and Column 20, lines 1-43 – State the following: "The following protocol is employed for intracage bus data transfers. During the request phase of the read cycle, the master requests access to either bus A or B of the intracage bus to read data from the local memory of any slave on the CBS. Upon being granted access by the bus arbitrator, the master transmits the address of the location to be read on the address bus of the DTB. All slaves capture that information after one clock cycle to determine whether they must respond. The addressed slave uses the transmitted address to access the specified location, and, upon completion of the read access, requests use of the same DTB. When such use is granted, the slave transmits the read data and acknowledges the successful completion of the access, also placing applicable address information for the master and itself into the transmitted data. The master then recognizes its address, checks the tag field to verify that the data is being received from the correct slave, and captures the data on the bus. When a*

master desires to write data into the local memory of a slave on the CBS, the master initiates a write cycle requesting access to bus A or B of the intracage bus. Upon being granted access by the ARB, the master transmits the address of the location into which the data is to be written on the address bus of the DTB. Here again, all slaves capture the information transmitted on the bus after one clock cycle, and determine from it whether they must respond to the bus cycle. The addressed slave uses the transmitted address to access the specified location, and when the write access is complete it will request use of the same DTB. Upon being granted use of the bus, the slave will acknowledge that the access was successfully completed. The slave places contents of the tag field identifying the master into address bits and its' cage and slot address into the tag field, so that the master can recognize its address, capture the data on the bus, and verify that the data was received from the correct slave. The master initiates the RMW cycle to read and possibly modify the contents of a location on the SSU without allowing that location to be written to by another card. The RMW bus cycle consists of a read cycle, possibly followed by a write cycle at a later time depending on the software code executed. The master requests access to bus A or B of the intracage bus and the same initial procedure is followed as was indicated above for the write cycle, except that the master also asserts the RMW signal on the backplane, indicating to the SSU that this is a read /modify/write bus cycle. The read and write bus cycles are performed according to the above description, and, while the RMW signal is asserted, the location accessed by the master is locked to preclude any card other than the master that initiated the RMW cycle from writing to the locked location. If another card attempts to write to that location, the request is blocked and held in the queue on the SSU until

the previous RMW cycle is completed. The deassertion of the RMW signal indicates completion of the RMW cycle")

- wherein said arbitration logic is associated with said read/write port and said arbitration logic routes a data access request requesting access of data in one portion of said at least one memory received from said memory access interface to one of said at least two buses providing access to said one portion of said at least one memory and routes a further data access request requesting access of data in a further portion of said at least one memory received from said data processing portion to a further one of said at least two buses providing access to said further portion of said at least one memory, said routing of said data access requests being performed during the same clock cycle. *(Column 6, lines 22-37 – State the following: "In a presently preferred embodiment, the utilization devices are designated as either master or slave modules, or both. A master module may initiate a bus cycle to access a slave, to transfer data between itself and the slave. A slave module has only the capability to respond to a request from a master to perform a particular bus cycle. Three types of bus cycles may be executed on the central bus system, consisting of read, write, and read/modify/write cycles, each cycle consisting of a request phase and a response phase. The bus system and the arbitration protocol are such that a requesting module (a master) will only drive the bus for one clock cycle, assuring a response to the access request within that cycle, and thereby enhancing the bus throughput by freeing the bus for other requesters" Column 24, lines 19-36 – State the following: "The SPCU interfaces to the PTB to provide communication with an associated LPM, the PTB interface connecting to the 32-bit PTB data bus and the 25-bit PTB address bus. Arbitration for access to the PTB is provided by the PTB interface located on the LPM. Operation of the SPCU as either a master or a slave on the PTB is permitted. In the*

former mode, an MC 68020 microprocessor on the SpCU may initiate data transfers on the PTB, whereas in the slave mode, external cards may access local memory and registers. The microprocessor operates at 12.5 MHz to transfer data between the resident serial ports and the LPM local RAM via the PTB; and, as in other units mentioned above having such microprocessors, it supports fully vectored interrupt handling, multiple bus master arbitration and a dynamic bus sizing capability that allows the processor to communicate with external devices of various data bus widths")

Claim 2. A data processing apparatus according to claim 1, said arbitration logic selecting one of said at least two buses to which said data access request is routed in dependence upon an address location within said at least one memory associated with said data access request. *(Column 20, lines 44-67 – State the following: "An ARB consists of the following primary functions: an intracage Bus Arbiter for DTB A and DTB B. and intercage Bus Arbiter, an intracage bus interface for DTB A and DTB B, an intercage bus interface, an intercage interface bus, a bus Clock Generator, a local bus interface, local bus functions, an LPM redundancy control port, and an Arbitrator control port. Arbitration for Intracage DTB A and B and Intercage DTB is performed in parallel on every bus cycle. A CBS interface chip is used at each interface to buffer the transfers between the intracage bus and the intercage bus. Parity is checked for data transfers through the ARB. The intercage interface bus connects the intercage bus interface and the interface to the intracage buses. The Intercage Bus Arbiter controls access to the intercage interface bus. The local bus includes the local bus interface, local bus address decoder, local bus hardware registers, system configuration storage, real time clock, and local bus control The local bus interface consists of a CBS interface chip set to buffer transfers between the local bus and the intracage DTBs. The local bus address decoder enables functions on the*

local bus. The local bus hardware registers provide control and status information on the ARB and the CBS. The system configuration storage consists of 2K bytes of battery backed RAM. The real time clock provides clock/calendar functions. The local bus control controls the data transfers on the local bus. The LPM redundancy control port transmits serially the control bits generated by the CPU to the RCB")

Claim 3. A data processing apparatus according to claim 2, wherein said at least two portions of said memory comprise an instruction portion storing instructions and at least one data portion storing data items, said arbitration logic routing said data access request to a first one of said at least two buses providing access to said instruction portion when data to be transferred is an instruction and routing said data access request to a second of said at least two buses providing access to said at least one data portion when data to be transferred is a data item. *(Column 29, lines 43-44 and Column 30, lines 1-27 – State the following: "A communication processor for a packet-switched network, comprising means for distributing data to and from transmission links of said network; at least one data communication bus means for transferring data internally of said processor in timed bus cycles; plural means for processing incoming data received by said distributing means from selected ones of said transmission links; plural means for storing data processed by said processing means; plural means for retrieving data for transmission thereof via said distributing means to selected ones of said transmission links; said at least one bus means interconnecting said plurality of processing means, storage means and retrieving means, whereby there is competition therebetween for data transfer via said at least one bus means during each of said bus cycles; and programmable means responsive to the degree of data traffic being handled by each of said processing means and said retrieving mean for selectively and continuously establishing a greater or lesser degree of access thereby to said bus means according to*

said respective degree of data traffic, whereby to alter access of said processing means, storage means and retrieving mean to said bus means during each bus cycle according to need for access")

Claim 5. A data processing apparatus according to claim 1, wherein said arbitration logic, in response to receipt of a data access request from said memory access interface portion and a data access request from said data processing portion, both data access requests requesting access to data in one portion of said at least one memory, routing said data access request from said memory access interface portion to one of said at least two buses providing data access to said one portion of said at least one memory before routing said request from said processing portion to said one of said at least two buses. *(Column 20, lines 44-67 – State the following: "An ARB consists of the following primary functions: an intracage Bus Arbiter for DTB A and DTB B. and intercage Bus Arbiter, an intracage bus interface for DTB A and DTB B, an intercage bus interface, an intercage interface bus, a bus Clock Generator, a local bus interface, local bus functions, an LPM redundancy control port, and an Arbitrator control port. Arbitration for Intracage DTB A and B and Intercage DTB is performed in parallel on every bus cycle. A CBS interface chip is used at each interface to buffer the transfers between the intracage bus and the intercage bus. Parity is checked for data transfers through the ARB. The intercage interface bus connects the intercage bus interface and the interface to the intracage buses. The Intercage Bus Arbiter controls access to the intercage interface bus. The local bus includes the local bus interface, local bus address decoder, local bus hardware registers, system configuration storage, real time clock, and local bus control The local bus interface consists of a CBS interface chip set to buffer transfers between the local bus and the intracage DTBs. The local bus address decoder enables functions on the local bus. The local bus hardware registers provide control and status information on the ARB and the CBS. The*

system configuration storage consists of 2K bytes of battery backed RAM. The real time clock provides clock/calendar functions. The local bus control controls the data transfers on the local bus. The LPM redundancy control port transmits serially the control bits generated by the CPU to the RCB")

Claim 6. A data processing apparatus according to claim 1, said arbitration logic detecting a wait request from at least one busy portion of said at least one memory, said arbitration logic not routing any data access requests to said busy portion until said wait request is no longer detected. *(Column 11, lines 55-68 and Column 12, lines 1-2 – State the following: "The arbitration scheme employed in packet switches according to the present invention assures that each time the ARB receives a bus request for a high priority group card, the ARB will issue a bus grant within one clock cycle when there is no contention for the bus requested. Hence, the bus protocol assures that the bus is being utilized to its full bandwidth. Unlike the prior art arbitration schemes in which a requester may be forced to wait until a token is passed to it before its request may be transmitted, or to wait through many clock cycles to accommodate some other protocol despite the possibility that it is the only requester, the presently preferred system allows any unit to request the bus at the instant access is desired and to be granted access within a reasonable time after the request is received by the ARB, depending on the assigned priority")*

Claim 7. A data processing apparatus according to claim 1, further comprising: at least one memory, said at least one memory being divided into at least two portions; and at least two buses, each bus allowing data access to a respective portion of said at least two portions of said at least one memory. *(Column 3,lines 42-46 – State the following: "Accordingly, the 8-bit parallel data is read out by the DMA controller 30 and the blocks of data are thereby transferred out on one of the two DAB buses 20 (A or B) and into a particular location in the main memory 10 (FIG. 1)")*

Claim 9. A data processing apparatus according to claim 7, wherein said at least one memory is a tightly coupled memory. *(Column 29, lines 43-44 and Column 30, lines 1-5 – State the following: "A communication processor for a packet-switched network, comprising means for distributing data to and from transmission links of said network; at least one data communication bus means for transferring data internally of said processor in timed bus cycles")*

Claim 10. A method of transferring data between an external data source and at least one memory associated with a data processor core, said data processor core comprising a memory access interface portion performing data transfer operations between said external data source and said at least one memory associated with said data processor core and a data processing portion performing data processing operations, said method comprising the steps of: *(Column 4, lines 3-66 – State the following: "Once data is transferred into the main memory 10, CPU 15 monitors that data and the intercard (i.e., LPUs and other units of the switch) communication areas, to determine where the data should now be transferred. The CPU then notifies an appropriate LPU that particular data in the main memory is to be transferred to that LPU. Accordingly, the path of data is via a modem through an LPU, with arbitration onto the bus and into main memory. Then a processing decision is made by the CPU as to the intra-switch destination for the data, and the CPU thereupon notifies the other card (the LPU), whereupon the data is transferred out of main memory through the selected LPU, its associated interface, and out through that modem or port. This is the manner in which the TP4000/II switch performs its packet switching. The packetizing (i.e., packet assembly) is accomplished in the LPU. Asynchronous data is received, packets are formed, and the packets are subsequently switched throughout the network until, at the other end, the packet is disassembled and transferred as asynchronous data again. The TP4000/II arbitration protocol on the DAB bus treats*

CPUs separately from LPUs. A block diagram useful for describing the protocol is shown in FIG. 3. The LPUs 40-1, 40-2, 40-n compete for access to the bus, in order to have their respective data packets (if any) read into the main memory. The competition is arbitrated by ARB unit 42 in a daisy chain approach by which the ARB initially passes a token to the LPU 40-1. If that LPU is ready to use the bus, it will hold the token and the bus, and on completion of its use will pass the token to the next LPU in the chain. If at that point LPU 40-2 has no need for access to the bus, it will simply pass the token to the next LPU. Finally, the last LPU in the chain, 40-n, passes the token back to the ARB 42. The scheme is such that the holder of the token holds possession of the bus. A separate token is employed for the CPUs 45-1 and 45-2, and here again a daisy chain approach is employed for the arbitration. If the CPUs are not using their bus time, the LPUs may use it. With this protocol, there may be passage of considerable time for the token to travel between units before the unit presently desiring to use the bus is encountered. That is, if LPU 40-1, for example, initially receives the token and has no present need to use the bus, the token is passed from LPU to LPU, When perhaps only LPU 40-15 is in need of access. Viewing the bus protocol of FIG. 3 in terms of clock cycles, a CPU or an LPU will remain idle and waiting until the token is passed to it--indeed, the unit may sit and wait until the token passes through a considerable number of LPUs until it finally gets the token--despite the fact that it may be the only card that is seeking to transfer data and, therefore, that requires the bus. Hence, time, and as a result, valuable bandwidth may be wasted as the token is passed from card to card until a need to use the bus is found. Moreover, as previously noted, at least some of the units within the packet switch, such as the LPUs, are individually configured on respective printed circuit cards. These cards are inserted into designated slots in cages within a console. The bus protocol requires that a ribbon cable be run between cages, with an

attendant further slowing of the bus." Column 24, lines 19-36 – State the following: "The SPCU interfaces to the PTB to provide communication with an associated LPM, the PTB interface connecting to the 32-bit PTB data bus and the 25-bit PTB address bus. Arbitration for access to the PTB is provided by the PTB interface located on the LPM. Operation of the SPCU as either a master or a slave on the PTB is permitted. In the former mode, an MC 68020 microprocessor on the SpCU may initiate data transfers on the PTB, whereas in the slave mode, external cards may access local memory and registers. The microprocessor operates at 12.5 MHz to transfer data between the resident serial ports and the LPM local RAM via the PTB; and, as in other units mentioned above having such microprocessors, it supports fully vectored interrupt handling, multiple bus master arbitration and a dynamic bus sizing capability that allows the processor to communicate with external devices of various data bus widths")

- in response to a data access request requesting access of data in one portion of said at least one memory received from said memory access interface portion and a data access request requesting access to data in a further portion of said at least one memory received from said data processing portion, routing said data access request received from said memory access interface portion to one of at least two buses, said one of said at least two buses providing access to said one portion of said at least one memory, and routing said data access request received from said data processing portion to a further of said at least two buses, said further bus providing access to said further portion of said at least one memory, said routing of said data access requests being performed during the same clock cycle. *(Column 6, lines 22-37 – State the following: "In a presently preferred embodiment, the utilization devices are designated as either master or slave modules, or both. A master module may initiate a bus cycle to access a slave, to transfer*

data between itself and the slave. A slave module has only the capability to respond to a request from a master to perform a particular bus cycle. Three types of bus cycles may be executed on the central bus system, consisting of read, write, and read/modify/write cycles, each cycle consisting of a request phase and a response phase. The bus system and the arbitration protocol are such that a requesting module (a master) will only drive the bus for one clock cycle, assuring a response to the access request within that cycle, and thereby enhancing the bus throughput by freeing the bus for other requesters")

Claim 11. A method according to claim 10, wherein said step of routing data access requests to respective data buses is done in dependence upon an address location within said at least one memory associated with said data access request. *(Column 20, lines 44-67 – State the following: "An ARB consists of the following primary functions: an intracage Bus Arbiter for DTB A and DTB B. and intercage Bus Arbiter, an intracage bus interface for DTB A and DTB B, an intercage bus interface, an intercage interface bus, a bus Clock Generator, a local bus interface, local bus functions, an LPM redundancy control port, and an Arbitrator control port. Arbitration for Intracage DTB A and B and Intercage DTB is performed in parallel on every bus cycle. A CBS interface chip is used at each interface to buffer the transfers between the intracage bus and the intercage bus. Parity is checked for data transfers through the ARB. The intercage interface bus connects the intercage bus interface and the interface to the intracage buses. The Intercage Bus Arbiter controls access to the intercage interface bus. The local bus includes the local bus interface, local bus address decoder, local bus hardware registers, system configuration storage, real time clock, and local bus control The local bus interface consists of a CBS interface chip set to buffer transfers between the local bus and the intracage DTBs. The local bus address decoder enables functions on the local bus. The local bus hardware registers provide control and status*

information on the ARB and the CBS. The system configuration storage consists of 2K bytes of battery backed RAM. The real time clock provides clock/calendar functions. The local bus control controls the data transfers on the local bus. The LPM redundancy control port transmits serially the control bits generated by the CPU to the RCB")

Claim 12. A method according to claim 10, wherein said at least two portions of said memory comprise an instruction portion storing instructions and at least one data portion storing data items, said step of routing said data access requests routing a data access request to one of said at least two buses providing access to said instruction portion when data to be transferred is an instruction and routing said data access request to another of said at least two buses providing access to said at least one data portion when data to be transferred is a data item. *(Column 29, lines 43-44 and Column 30, lines 1-27 – State the following: "A communication processor for a packet-switched network, comprising means for distributing data to and from transmission links of said network; at least one data communication bus means for transferring data internally of said processor in timed bus cycles; plural means for processing incoming data received by said distributing means from selected ones of said transmission links; plural means for storing data processed by said processing means; plural means for retrieving data for transmission thereof via said distributing means to selected ones of said transmission links; said at least one bus means interconnecting said plurality of processing means, storage means and retrieving means, whereby there is competition therebetween for data transfer via said at least one bus means during each of said bus cycles; and programmable means responsive to the degree of data traffic being handled by each of said processing means and said retrieving mean for selectively and continuously establishing a greater or lesser degree of access thereby to said bus means according to said respective degree of data traffic, whereby to alter access of said processing means, storage*

means and retrieving mean to said bus means during each bus cycle according to need for access")

Claim 14. A method according to claim 10, wherein said routing step in response to receipt of a data access request from said memory access interface portion and a data access request from said data processing portion, both data access requests requesting access to data in a portion of said at least one memory accessed by one of said at least two buses, routes said data access request from said memory access interface portion to said one of said at least two buses before routing said request from said processing portion to said one of said at least two buses. *(Column 20, lines 44-67 – State the following: "An ARB consists of the following primary functions: an intracage Bus Arbiter for DTB A and DTB B. and intercage Bus Arbiter, an intracage bus interface for DTB A and DTB B, an intercage bus interface, an intercage interface bus, a bus Clock Generator, a local bus interface, local bus functions, an LPM redundancy control port, and an Arbitrator control port. Arbitration for Intracage DTB A and B and Intercage DTB is performed in parallel on every bus cycle. A CBS interface chip is used at each interface to buffer the transfers between the intracage bus and the intercage bus. Parity is checked for data transfers through the ARB. The intercage interface bus connects the intercage bus interface and the interface to the intracage buses. The Intercage Bus Arbiter controls access to the intercage interface bus. The local bus includes the local bus interface, local bus address decoder, local bus hardware registers, system configuration storage, real time clock, and local bus control The local bus interface consists of a CBS interface chip set to buffer transfers between the local bus and the intracage DTBs. The local bus address decoder enables functions on the local bus. The local bus hardware registers provide control and status information on the ARB and the CBS. The system configuration storage consists of 2K bytes of battery backed RAM. The real time clock provides clock/calendar*

functions. The local bus control controls the data transfers on the local bus. The LPM redundancy control port transmits serially the control bits generated by the CPU to the RCB")

Claim 15. A method according to claim 10, said routing step detecting a wait request from at least one busy portion of said at least one memory, and in response to detection of said wait request not routing any data access requests to said busy portion until said wait request is no longer detected. *(Column 11, lines 55-68 and Column 12, lines 1-2 – State the following: "The arbitration scheme employed in packet switches according to the present invention assures that each time the ARB receives a bus request for a high priority group card, the ARB will issue a bus grant within one clock cycle when there is no contention for the bus requested. Hence, the bus protocol assures that the bus is being utilized to its full bandwidth. Unlike the prior art arbitration schemes in which a requester may be forced to wait until a token is passed to it before its request may be transmitted, or to wait through many clock cycles to accommodate some other protocol despite the possibility that it is the only requester, the presently preferred system allows any unit to request the bus at the instant access is desired and to be granted access within a reasonable time after the request is received by the ARB, depending on the assigned priority")*

Claim 17. Arbitration logic controlling a data processor to perform the steps of the method according to claim 10. *(Column 5, lines 31-37 – State the following: "A more specific object of the invention is to provide a packet switch, or communication processor, utilizing an improved arbitration scheme that allows any data processor (e.g, packet assembler/disassembler (PAD), CPU, and so forth) to request the bus immediately upon need for access and to have that need assessed within a brief time interval such a single clock cycle")*

Claim 18. A data processing apparatus according to claim 1, wherein said data processor core comprises said arbitration logic. *(Column 5, lines 31-37 –*

State the following: "A more specific object of the invention is to provide a packet switch, or communication processor, utilizing an improved arbitration scheme that allows any data processor (e.g, packet assembler/disassembler (PAD), CPU, and so forth) to request the bus immediately upon need for access and to have that need assessed within a brief time interval such a single clock cycle")

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 8, 13, and 16 are rejected under 35 U.S.C.103(a) as being unpatentable over Makris et al. as applied to claims 1-3, 7, 10, and 12 above, further in view of Tamura et al. (US PGPub 2003/0033573 A1).

Makris teaches the limitations of claims 1-3, 7, 10, and 12 for the reasons above.

Makris' invention differs from the claimed invention in that there is no specific reference to a odd or even addresses or where they are stored.

Makris fails to teach claims 4, 8, 13, and 16, which respectively state the following:

Claim 4. A data processing apparatus according to claim 3, wherein said at least one data portion comprises two data portions, an even data portion storing data having an even address and an odd data portion storing data having an odd address, said read/write port transferring data between said processor core and said at least one memory via three buses, a first bus providing access to said instruction portion, a second bus providing access to said odd data portion and a third bus providing access to said even data portion, and said arbitration logic routing a data access request to said first bus when data to be transferred is an instruction, to said second bus when

data to be transferred is a data item associated with an odd address and to said third bus when data to be transferred is a data item associated with an even address.

Claim 8. A data processing apparatus according to claim 7, wherein said at least one memory is divided into three portions, an instruction portion storing instructions, and two data portions, an even data portion storing data having an even address and an odd data portion storing data having an odd address, said data processing apparatus comprising three buses said read/write port transferring data between said processor core and said at least one memory via said three buses, a first bus providing access to said instruction portion, a second bus providing access to said odd data portion and a third bus providing access to said even data portion.

Claim 13. A method according to claim 12, wherein said at least one data portion comprises two data portions, an even data portion storing data having an even address and an odd data portion storing data having an odd address, said routing step routing data accesses to one of three buses, a first bus providing access to said instruction portion, a second bus providing access to said odd data portion and a third bus providing access to said even data portion, and said routing step routing a data access request to said first bus when data to be transferred is an instruction, to said second bus when data to be transferred is a data item associated with an odd address and to said third bus when data to be transferred is a data item associated with an even address.

Claim 16. A method according to claim 10, wherein said at least one memory is divided into three portions, an instruction portion storing instructions, and two data portions, an even data portion storing data having an even address and an odd data portion storing data having an odd address, said routing step routing a received data access request to one of three buses, a first bus providing access to said instruction portion, a second bus providing access to said odd data portion and a third bus providing access to said even data portion, in dependence upon an address of said data associated with said data access request.

However, Tamura's invention discloses the following: "For example, in the flash memory 2 of FIG. 3, the data part PrtD of the sector address SA1 contains even byte data of the sector data 2n (even byte data in each byte data of, for example 512 bytes) EvD (2n), ECC code EvC (n2) as an error detection code relating to even byte data of the sector data 2n, even byte data of the sector data 2n+1 (even 256 byte data in each byte data in each byte data of, for example 512 bytes) EvD (2n+1), and an ECC code EvC (2n+1) as an error detection code

relating to even byte data of the sector data 2n+1. The management part PrtM of the sector address SA1 (n) has a good sector code, identification information, other management information and ECC code as management information of the sector address n. The good sector code is a code data representative of whether the sector address SA1 (n) is good or not. The identification code is a code data representative of which of the user data, alternated area, vacant area, or alternate area management area, the corresponding data part belongs to. The other management information may not be particularly defined. The ECC code is error detection and correction redundancy information for good sector code, identification information and other management information. In the flash memory 3 of FIG. 4, the data part PrtD of the sector address SA2 (n) contains odd byte data of the sector data 2n (odd 256 byte data in each byte data of, for example, 512 bytes) OdD (2n), ECC code EvC (2n) as the error detection code relating to odd byte data of the sector data 2n, odd byte data of the sector data 2n+1 (odd 256 byte data in each byte data of, for example, 512 bytes), OdD (2n+1) and ECC code OdC (2n+1) as the error detection code relating to odd byte data of the sector data 2n+1. The management information which the management part PrtM of the flash memory 3 possesses has meaning which is similar to that of the flash memories of FIG. 3" (Sections 0061-0062). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Communication Processor for a Packet-Switched Network" of Makris and Tamura's "Memory Card and Memory Controller" before him at the time the invention was made, to combine the inventions to allow for there to be a portion for odd and even data address storage to enhance system efficiency.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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